

04-03-06

Attorney Docket: 1346P/DA01028

PATENT

THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, DC 20231

00/03/00
Inventors:
For:
C. S. PTO

Transmitted herewith for filing is a Patent Application in the name of:

Mark S. Chang; Hao Fang; and King Wai Kelwin Ko

**METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER
A FLASH MEMORY DEVICE**

Enclosed with the Patent Application are:

- Five (5) sheet(s) of drawings
- Declaration of Inventor(s)
- Power of Attorney by Assignee
- Assignment and Recordation Form
- Information Disclosure Statement (PTO Form 1449)
- Self Addressed, Stamped Postcard

The filing fee has been calculated as shown below:

(Col. 1)	(Col. 2)			
FOR:	NO. FILED	NO. EXTRA		
<hr/> BASIC FEE				
<hr/> TOTAL CLAIMS				
16	-	20	=	0
<hr/> INDEP. CLAIMS				
2	-	3	=	0
<hr/> MULTIPLE DEPENDENT CLAIM PRESENTED				

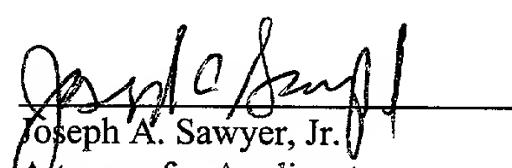
*If the difference in Col. 1 is less than "0", enter "0" in Col. 2

LARGE ENTITY	
RATE	FEE
<hr/> \$ 690.00	
x 18 =	\$ 0.00
<hr/> \$ 0.00	
x 78 =	\$ 0.00
<hr/> \$ 0.00	
TOTAL	\$ 690.00

- The Commissioner is hereby authorized to charge payment of \$ 690.00 and the following fees associated with this communication or credit any overpayment to Deposit Account 01-0365. A duplicate copy of this sheet is attached.
- Any additional filing fees required under 37 CFR 1.16.
- Any patent application processing fees under 37 CFR 1.17.

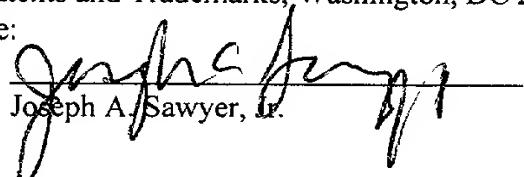
SAWYER LAW GROUP LLP
Post Office Box 51418
Palo Alto, California 94303
(650) 493-4540

Respectfully submitted,


Joseph A. Sawyer, Jr.
Attorney for Applicant
Reg. No. 30,801

EXPRESS MAIL CERTIFICATE

I hereby certify that the above paper/fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to the Commissioner of Patents and Trademarks, Washington, DC 20231, on **March 30, 2000**. Express Mail No.: **EL547854460US**. Signature of Person mailing paper/fee:


Joseph A. Sawyer, Jr.

1025 U. S. P. T. O.
109/539458
03/30/00

UNITED STATES PATENT APPLICATION

FOR

METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST
POLYSILICON LAYER IN A FLASH MEMORY DEVICE

Inventors:

Mark S. Chang
Hao Fang
King Wai Kelwin Ko

Sawyer Law Group, LLP
2465 E. Bayshore Road Suite 406
Palo Alto, California 94303

METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE

FIELD OF THE INVENTION

The present invention relates to flash memory devices, and more particularly to a method and system for providing contacts to the first polysilicon layer in the flash memory devices.

5

BACKGROUND OF THE INVENTION

Flash memory devices are a popular form of nonvolatile storage. Flash memory devices can retain information when no power is supplied to the device. Flash memory devices include memory cells that include a gate stack, a source and a drain. Each gate stack also includes a control gate separated from the floating gate by an insulating layer. The insulating layer is typically a composite ONO layer including two oxide layers separated by a nitride layer. The control gate and the floating gate are typically formed of polysilicon. Some memory cells may be separated by field oxide regions. Contact is made to the source and drain regions as well as to the gate stacks

15 In conventional flash memory devices, particularly in NAND technology, it may be desirable to provide other components using one of the polysilicon layers which form the floating gate and control gate. For example, the first polysilicon layer may be used to form resistors or other components for the flash memory device. Consequently, contacts are desired to be provided to the gate stacks, the source and drain regions and the components 20 comprised of the first polysilicon layer.

Figure 1 depicts a conventional method for providing a conventional flash memory

device, such as a NAND device, that includes components, other than the gate stacks, which use one of the polysilicon layers. For clarity, it is assumed that the first polysilicon layer is used. Such components will also be called poly-1 components. The gate stacks, source and drain regions and poly-1 components are formed, via step 12. Typically, step 12 includes forming field oxide regions, depositing a first polysilicon layer, forming the ONO layer, patterning the ONO and first polysilicon layers, depositing a second polysilicon layer with the poly-1 component already patterned, and etching the second polysilicon layer and ONO layer to form the gate stacks and the poly-1 component. Step 12 also typically includes implanting the source and drain regions. From the perspective of contact formation, source and drain regions are similar. Consequently, all such regions are referred to as source/drain regions. Often, step 12 also includes forming a silicide, usually a tungsten-silicide, on the gate stacks and providing a capping layer including SiON on the gate stack.

An insulating layer is then formed, via step 14. The insulating layer covers the source/drain regions, the gate stacks, the field oxide regions and the poly-1 components. Contact holes are then etched, via step 16, to allow electrical contact to the gate stacks, the source/drain regions, and the poly-1 components. Typically, the contact holes for the gate stacks, the source/drain regions, and the poly-1 components are etched simultaneously. The contact holes may then be filled with a conductive material, via step 18.

Although the conventional method 10 functions, one of ordinary skill in the art will readily realize that it is difficult to provide contact to the poly-1 components using the conventional method 10. Figures 2A and 2B depict a conventional flash memory device 50 fabricated using the conventional method 10. Figure 2A depicts the conventional flash memory device 50 prior to formation of contact holes. The conventional flash memory

device 50 includes a substrate 52 on which a gate stack 60, source/drain regions 56 and 58, oxide layer 55 and field oxide 54 are formed. The gate stack 60 includes a floating gate 62, an insulating layer 64, a control gate 66, a tungsten silicide layer 68 and a SiON layer 70. Spacers 72 and 74 can be formed on opposite sides of the gate stack 60. The floating gate 62 and control gate 66 are formed from first and second polysilicon layers, respectively. The insulating layer 64 is typically an ONO layer 64, which includes two layers of oxide separated by a nitride layer. Also depicted is a poly-1 component 76 which includes a polysilicon layer 76 and happens to be located on the field oxide region 54. On the poly-1 component 76 is an ONO layer 78. The poly-1 component 76 may be formed using the first polysilicon layer. Similarly, the ONO layer 78 may be formed using the same ONO layer that forms the ONO layer 64. Blanketing the gate stack 60, the source/drain regions and the poly-1 component is an insulating layer 80, which is typically formed of oxide.

Figure 2B depicts the conventional flash memory device 50 after the contact holes have been etched using step 16 of the method 10. Referring back to Figure 2B, the contact holes 82, 84, and 86 are of very different **depths**. The contact hole 82 to the gate stack 60 is the shallowest. The contact hole 84 to the source/drain region 56 is the deepest. The contact hole 86 to the poly-1 component 76 has a medium depth. Typically, the contact holes 82, 84 and 86 are etched concurrently. Furthermore, because the percentage of area occupied by the contact holes 82, 84 and 86 is small, endpoint detection using conventional techniques is difficult. Consequently, some overetch is usually performed.

Because of the etch used to form the contact hole 82, 84 and 86, the poly-1 component 76 may be destroyed. The tungsten silicide layer 68 prevents the gate stack 60 from being etched through. The source/drain region 56 is the deepest to which contact is

made and the etch stops at the silicon. Thus, the etch does not substantially harm the source/drain region 56. However, the poly-1 component 76 and the ONO layer 78 have been etched partially or wholly through. Consequently, the poly-1 component may be destroyed. The etch may even remove the field oxide region 54 under the poly-1 component 76. Removal of the field oxide region 54 could expose the underlying silicon substrate 52, which is undesirable. The conventional flash memory device 50 may, therefore, not operate as desired.

Accordingly, what is needed is a system and method for providing contacts to the poly-1 components without destroying the poly-1 components or underlying structures. The present invention addresses such a need.

SUMMARY OF THE INVENTION

The present invention provides a method and system for providing at least one contact in a flash memory device. The flash memory device includes a plurality of gate stacks and at least one component including a polysilicon layer having a top surface. The method and system comprise forming a silicide on the top surface of the polysilicon layer and forming an insulating layer covering the plurality of gate stacks, the at least one component and the silicide. The method and system also comprise etching the insulating layer to provide at least one contact hole. The insulating layer etching step uses the silicide as an etch stop layer to ensure that the insulating layer etching step does not etch through the polysilicon layer. The method and system also comprise filling the at least one contact hole with a conductor.

According to the system and method disclosed herein, the present invention allows

contact to be more easily made to components which are made from the first polysilicon layer.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Figure 1 is a flow-chart of a conventional method for forming contacts in a flash memory device.

Figure 2A is a diagram of a conventional flash memory device having a first polysilicon layer device prior to formation of contact holes.

10 Figure 2B is a diagram of a conventional flash memory device having a first polysilicon layer device after formation of contact holes.

Figure 3A is a flow chart of one embodiment of method in accordance with the present invention for providing contacts in a flash memory device.

15 Figure 3B is a diagram of one embodiment of a flash memory device in accordance with the present invention.

Figure 4 is a flow chart depicting another embodiment of a method in accordance with the present invention for providing contacts in a flash memory device.

20 Figure 5A is a flow chart of another embodiment of method in accordance with the present invention for providing contacts in a flash memory device.

Figure 5B is a diagram of another embodiment of a flash memory device in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to an improvement in providing contacts in flash memory devices. The following description is presented to enable one of ordinary skill in

the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be applied to other embodiments. Thus, the present invention is not intended to be limited to the embodiment shown, but is to be accorded the widest scope consistent with the principles and features described herein.

Conventional flash memory devices are used for nonvolatile storage. It is desirable, for example in NAND technology, to utilize either the first or the second polysilicon layer for devices other than gate stacks. These devices which utilize the first polysilicon layer will be termed poly-1 components. However, one of ordinary skill in the art will readily realize that when contacts to the source/drain regions, the gate stacks and the poly-1 components are formed, the etch of the contact holes may destroy the poly-1 components and underlying structures, such as field oxides. Destruction of these portions of the flash memory device is undesirable.

The present invention provides a method and system for providing at least one contact in a flash memory device. The flash memory device includes a plurality of gate stacks and at least one component including a polysilicon layer having a top surface. The method and system comprise forming a silicide on the top surface of the polysilicon layer and providing an insulating layer covering the plurality of gate stacks, the at least one component and the silicide. The method and system also comprise etching the insulating layer to provide at least one contact hole. The insulating layer etching step uses the silicide to ensure that the insulating etching step does not etch through the polysilicon layer. The method and system also comprise filling the at least one contact hole with a conductor.

The present invention will be described in terms of a particular flash memory cell having certain components. However, one of ordinary skill in the art will readily recognize that this method and system will operate effectively for flash memory cells having other components. The present invention will also be described in the context of certain methods for fabricating the flash memory device. However, one of ordinary skill in the art will readily realize that the method and system will operate for other fabrication methods. For the purpose of clarity, the present invention will also be described in the context of methods in which certain steps are omitted. However, one of ordinary skill in the art will readily realize that other steps may be used. The present invention is also discussed in the context of specific materials. One of ordinary skill in the art, however, will readily realize that the present invention is consistent with the use of other materials. For example, although termed field oxide regions, such regions can be made of insulating materials other than an oxide.

To more particularly illustrate the method and system in accordance with the present invention, refer now to Figure 3A, depicting one embodiment of a method 100 in accordance with the present invention for providing contact to at least poly-1 components. The method preferably commences after gate stacks, source/drain regions and the poly-1 components have been formed. The method 100 also preferably commences when the top surface of the polysilicon layer in the poly-1 component is clean and relatively free from surface oxides. A silicide is formed on at least the polysilicon layer of the poly-1 components, via step 102. Step 102 is preferably performed using a self-aligned silicide (“salicide”) process. The silicide formed is preferably either a cobalt silicide or a titanium silicide. Titanium silicide may be desirable because the silicide can form despite a thin layer of oxide on a polysilicon

layer. However, the cobalt silicide may also be desirable because the resistivity of the cobalt silicide is lower than that of tungsten silicide.

An insulating layer is formed over the poly-1 components, the gate stacks and the source-drain regions, via step 104. Contact holes are then etched, via step 106. Etching step 5 uses the silicide layer formed in step 102 to prevent the poly-1 components from being etched through. The silicide layer is etched much slower than the insulating layer, which is usually an oxide. Preferably, the contact holes to the poly-1 components, the source/drain regions and the gate stacks are preferably etched concurrently. The silicide layer on the surface of the poly-1 component thus acts as an etch-stop layer and prevents damage to the poly-1 component even though overetching is performed and contact holes deeper than those to the poly-1 components are also formed. The contact holes are then filled with a conductor, via step 108. The silicide formed in step 102 aids in providing good electrical contact to the poly-1 components as well as protecting the poly-1 components during the contact hole etch.

15 Figure 3B depict one embodiment of a flash memory device 200 formed in accordance with the present invention. The flash memory device 200 includes a substrate 202 on which a gate stack 210, source/drain regions 206 and 208, oxide layer 205 and field oxide 204 are formed. The gate stack 210 includes a floating gate 212, an insulating layer 214, a control gate 216, an optional silicide layer 218 and a SiON layer 220. The silicide layer 218 may be a tungsten, titanium or cobalt silicide. Spacers 222 and 224 can be formed 20 on opposite sides of the gate stack 210. The floating gate 212 and control gate 216 are formed from first and second polysilicon layers, respectively. The insulating layer 214 is typically an ONO layer 214, which includes two layers of oxide separated by a nitride layer.

Also depicted is a poly-1 component 226 which includes a polysilicon layer 226 and happens to be located on the field oxide region 204. In a preferred embodiment, the poly-1 component 226 would be formed using the first polysilicon layer. However, another layer of polysilicon could be used. On the poly-1 component 226 is a silicide layer 228 formed in accordance with the present invention. Blanketing the gate stack 210, the source/drain regions 206 and 208 and the poly-1 component 226 is an insulating layer 230, which is generally formed of oxide. Contact holes 232, 234 and 236 have been etched into the insulating layer 230.

The contact holes 232, 234 and 236 have different depths. Furthermore, some overetch may have been performed to ensure that the contacts 232, 234 and 236 are to the desired depths. Because of the presence of the silicide layer 228, the poly-1 component 226 has not been etched during formation of the contact hole 236. Consequently, the poly-1 component 226 is still usable. Furthermore, the underlying field oxide region 204 remains intact. The silicide layer 228 also allows for better electrical contact to the poly-1 component 226 when a conductor (not shown) fills the contact hole 236. Furthermore, overetching can be performed to ensure that the contact holes 232, 234 and 236 also have the desired depth. Thus, the poly-1 components 226 can be used and the flash memory device 200 is operational.

Figure 4 depicts a more detailed flow chart of another embodiment of a method 110 for providing contacts to poly-1 components in accordance with the present invention. The method 110 preferably commences after formation of the poly-1 components, the gate stacks, the source drain regions, and the field oxide regions. The poly-1 component is often formed using the first polysilicon layer. A composite ONO layer generally covers the first

polysilicon layer. When the poly-1 components are formed, therefore, they are covered by the ONO layer. The method 110, therefore commences by removing the ONO layer from the poly-1 components when the second polysilicon layer is etched to form the control gates, via step 112. The removal of the ONO layer during the second polysilicon layer etch should be performed carefully to ensure that any oxide above the source/drain regions is not completely removed. In an alternate embodiment, the ONO layer on the poly-1 components could be removed separately from the etch of the second polysilicon layer. For example, after the second polysilicon layer is etched forming the gate stacks, the active areas could be masked, and the ONO layer on the poly-1 components removed separately.

A silicide is then formed on the exposed surface of the polysilicon layer of the poly-1 component, via step 114. In a preferred embodiment, the silicide layer is formed using a salicide process. The silicide formed is preferably a cobalt silicide or a titanium silicide. Titanium silicide may be desirable because the silicide can form despite a thin layer of oxide on a polysilicon layer. However, the cobalt silicide may also be desirable because the resistivity of the cobalt silicide is lower than that of titanium silicide. In a preferred embodiment, a silicide is formed on both the poly-1 component and on the second polysilicon layer, or control gate, of the gate stack in step 114. As a result, a separate step for forming titanium silicide on the gate stack may be omitted. However, also in a preferred embodiment no silicide is formed on the source/drain regions to prevent the source/drain regions from shorting to the gate stacks.

An insulating layer is formed over the poly-1 components, the gate stacks and the source-drain regions, via step 116. Contact holes are then etched, via step 118. Etching step uses the silicide layer formed in step 114 to prevent the poly-1 components from being

etched through. The silicide layer is etched much slower than the insulating layer, which is usually an oxide. Preferably, the contact holes to the poly-1 components, the source/drain regions and the gate stacks are preferably etched concurrently. The silicide layer on the surface of the poly-1 component thus prevents damage to the poly-1 component even though overetching is performed and contact holes deeper than those to the poly-1 components are also formed. The contact holes are then filled with a conductor, via step 120. The silicide formed in step 102 aids in providing good electrical contact to the poly-1 components as well as protecting the poly-1 components during the contact hole etch.

Figure 5A depicts another embodiment of a method 150 for providing contacts to a poly-1 component in a flash memory device. As in the method 110 described in Figure 4, the method 150 preferably commences after formation of the poly-1 components, the layers forming the gate stacks, the source/drain regions, and the field oxide regions. The poly-1 component is often formed using the first polysilicon layer. A composite ONO layer generally covers the first polysilicon layer. When the poly-1 components are formed, therefore, they are covered by the ONO layer. The second polysilicon layer is etched to form the control gates of the gate stacks, via step 152. Spacers are then formed along edges of the gate stack, via step 154. The spacers formed in step 154 are insulating spacers. The ONO layer on the poly-1 components and, in a preferred embodiment, the oxide layer on certain source/drain regions is removed, via step 156. Preferably, step 156 includes etching the ONO layer and the oxide layer. A silicide is formed on the poly-1 components, via step 158. In a preferred embodiment, a silicide layer is also formed on the tops of the gate stacks on the source/drain regions in step 158. The silicide layer is preferably formed using a salicide process. An insulating layer is then formed, via step 160. The insulating layer

covers the poly-1 components, the gate stacks, the source/drain regions, field oxide regions and the corresponding silicide layers. Contact holes are etched in the insulating layer, via step 162.

Figure 5B depict one embodiment of a flash memory device 250 formed in accordance with the method 150. The flash memory device 250 includes a substrate 252 on which a gate stack 260, source/drain regions 256 and 258, oxide layer 255 and field oxide 254 are formed. The gate stack 260 includes a floating gate 262, an insulating layer 264, and a control gate 266. Spacers 268 and 270 can be formed on opposite sides of the gate stack 260. The floating gate 262 and control gate 266 are formed from first and second polysilicon layers, respectively. The insulating layer 264 is typically an ONO layer. Also depicted is a poly-1 component 272 which includes a polysilicon layer 272 and happens to be located on the field oxide region 254. In a preferred embodiment, the poly-1 component 272 would be formed using the first polysilicon layer. However, another layer of polysilicon could be used. On the poly-1 component 272 is a silicide layer 274 formed in accordance with the present invention. In addition, the silicide layer 274 covers source/drain region 236 and control gate 266. However, because the silicide layer 274 was formed after the spacers 268 and 270, the silicide layer 274 on the source/drain region 256 will not short the source drain region 256 to the gate stack 260. Blanketing the gate stack 260, the source/drain regions 256 and 258 and the poly-1 component 272 is an insulating layer 278, which is generally formed of oxide. Contact holes 280, 282 and 284 have been etched into the insulating layer 278.

The contact holes 280, 282 and 284 have different depths. Furthermore, some overetch may have been performed to ensure that the contacts 280, 282 and 284 are to the

desired depths. Because of the presence of the silicide layer 274, the poly-1 component 272 has not been etched during formation of the contact hole 284. Consequently, the poly-1 component 272 is still usable. Furthermore, the underlying field oxide region 254 remains intact. The silicide layers 274 also allows for better electrical contact to the poly-1 component 272, the source/drain region 256 and the gate stack 260 when a conductor (not shown) fills the contact holes 280, 282, and 284. Furthermore, overetching can be performed to ensure that the contact holes 280, 282 and 284 also have the desired depth. Thus, the poly-1 components 272 can be used and the flash memory device 250 is operational. Moreover, good contact can be made relatively easily to the source/drain region 256 and the gate stack 260 in addition to the poly-1 component because of the presence of the silicide layer 274.

A method and system has been disclosed for providing contacts to a poly-1 component in a flash memory device. Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A flash memory device comprising:
2 a plurality of gate stacks including a plurality of floating gates and a plurality of
3 control gates disposed on a semiconductor substrate;
4 at least one component including a polysilicon layer having a top surface;
5 a silicide on the top surface of the polysilicon layer of the at least one component;
6 an insulating layer covering the plurality of gate stacks, the at least one component
7 and the silicide, the insulating layer having a plurality of contact holes therein, the plurality
8 of contact holes being formed by etching the insulating layer to provide the plurality of
9 contact holes, the insulating layer etching step using the silicide as an etch stop layer to
10 ensure that the insulating etching step does not etch through the polysilicon layer; and
11 a conductor for filling the plurality of contact holes.

1. The flash memory device of claim 1 wherein the silicide further includes a
2 titanium silicide.

1. The flash memory device of claim 1 wherein the silicide further includes a
2 cobalt silicide.

1. The flash memory device of claim 1 wherein the component further includes
2 an oxide-nitride-oxide layer on the polysilicon layer and wherein the oxide-nitride-oxide

3 layer is removed prior to formation of the silicide.

1 5. The flash memory device of claim 4 wherein the oxide-nitride-oxide layer is
2 removed during a second polysilicon layer etching step which forms the plurality of gate
3 stacks.

1 6. The flash memory device of claim 4 wherein the plurality of gate stacks
2 further include a plurality of spacers and wherein the oxide-nitride-oxide layer is removed
3 after formation of the plurality of spacers.

1 7. The flash memory device of claim 1 further comprising:
2 at least one field oxide region, the at least one component being located on the at
3 least one field oxide region.

1 8. A method for providing at least one contact in a flash memory device, the
2 flash memory device including a plurality of gate stacks and at least one component
3 including a polysilicon layer having a top surface, the method comprising the steps of:

4 (a) forming a silicide on the top surface of the polysilicon layer;
5 (b) providing an insulating layer covering the plurality of gate stacks, the at least
6 one component and the silicide;
7 (c) etching the insulating layer to provide at least one contact hole, the insulating
8 layer etching step using the silicide as an etch stop layer to ensure that the insulating etching
9 step does not etch through the polysilicon layer;

10 (d) filling the at least one contact hole with a conductor.

1 9. The method of claim 8 wherein the at least one contact hole further includes a
2 plurality of contact holes, wherein a plurality of source/drain regions are adjacent to the
3 plurality of gate stacks, and wherein the insulating layer etching step (c) further includes the
4 steps of:

5 (c1) etching the insulating layer to expose a portion of the plurality of gate stacks
6 in a first portion of the plurality of contact holes, to expose a portion of the plurality of
7 source/drain regions in a second portion of the plurality of contact holes and to expose the
8 silicide on the at least one polysilicon device in a third portion of the plurality of contact
9 holes.

10. The method of claim 8 wherein the silicide further includes a titanium
1 silicide.

11. The method of claim 8 wherein the silicide further includes a cobalt silicide.

12. The method of claim 8 wherein the component further include an oxide-
2 nitride-oxide layer on the polysilicon layer and wherein the method further includes the step
3 of:

4 (e) removing the oxide-nitride-oxide layer prior to formation of the silicide.

13. The method of claim 12 wherein the oxide-nitride-oxide layer removing step

2 (e) further includes the step of:

3 (e1) removing the oxide-nitride-oxide layer during a polysilicon layer etching step
4 which forms the plurality of gate stacks.

1 14. The method of claim 12 wherein the plurality of gate stacks further include a
2 plurality of spacers and wherein the oxide-nitride-oxide layer removing step (e) further
3 includes the step of:

4 (e1) removing the oxide-nitride-oxide layer after formation of the plurality of
5 spacers.

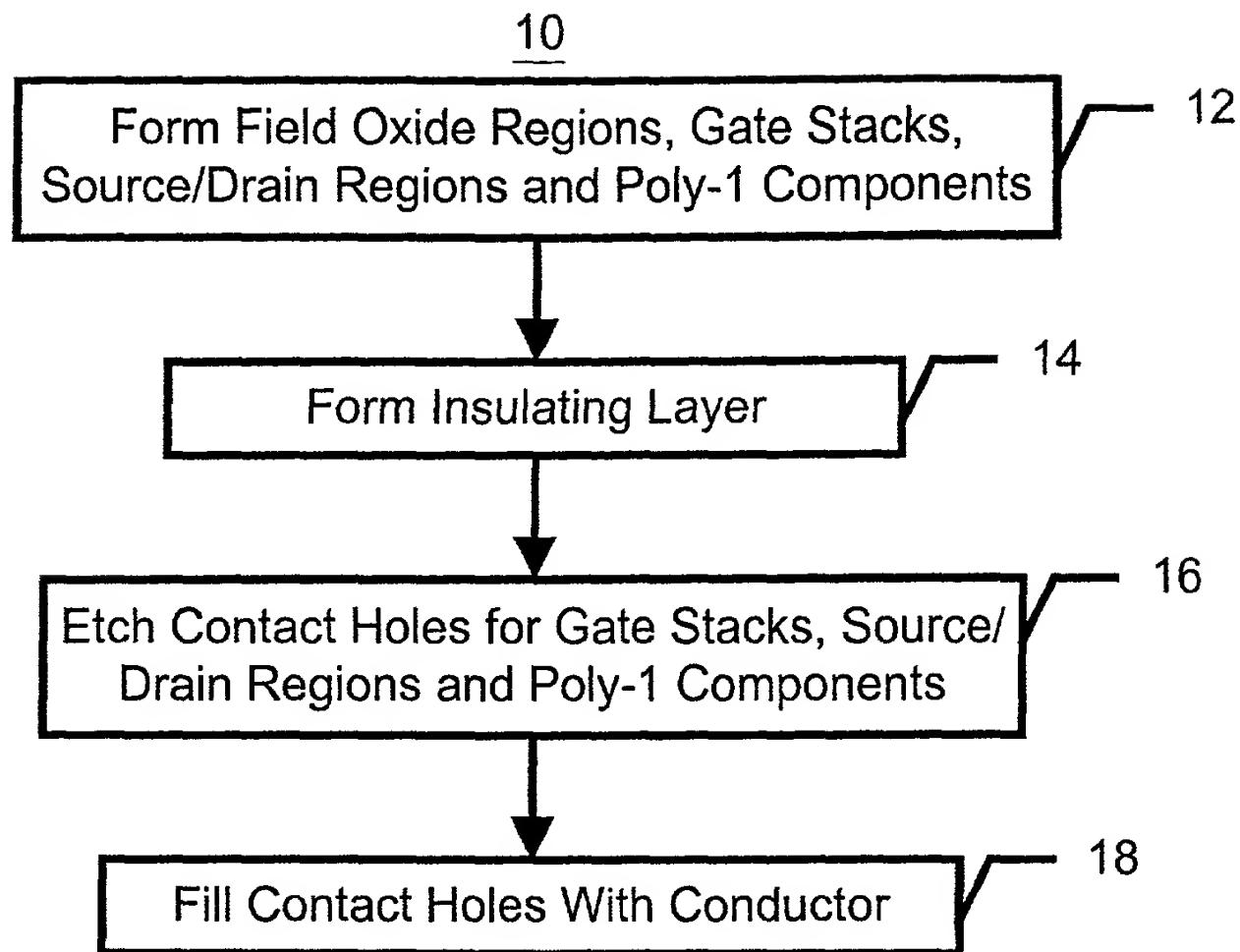
1 15. The method of claim 8 wherein the flash memory device further includes at
2 least one field oxide region, the at least one component being located on the at least one field
3 oxide region.

1 16. The method of claim 8 wherein the silicide forming step (a) further includes
2 the step of:

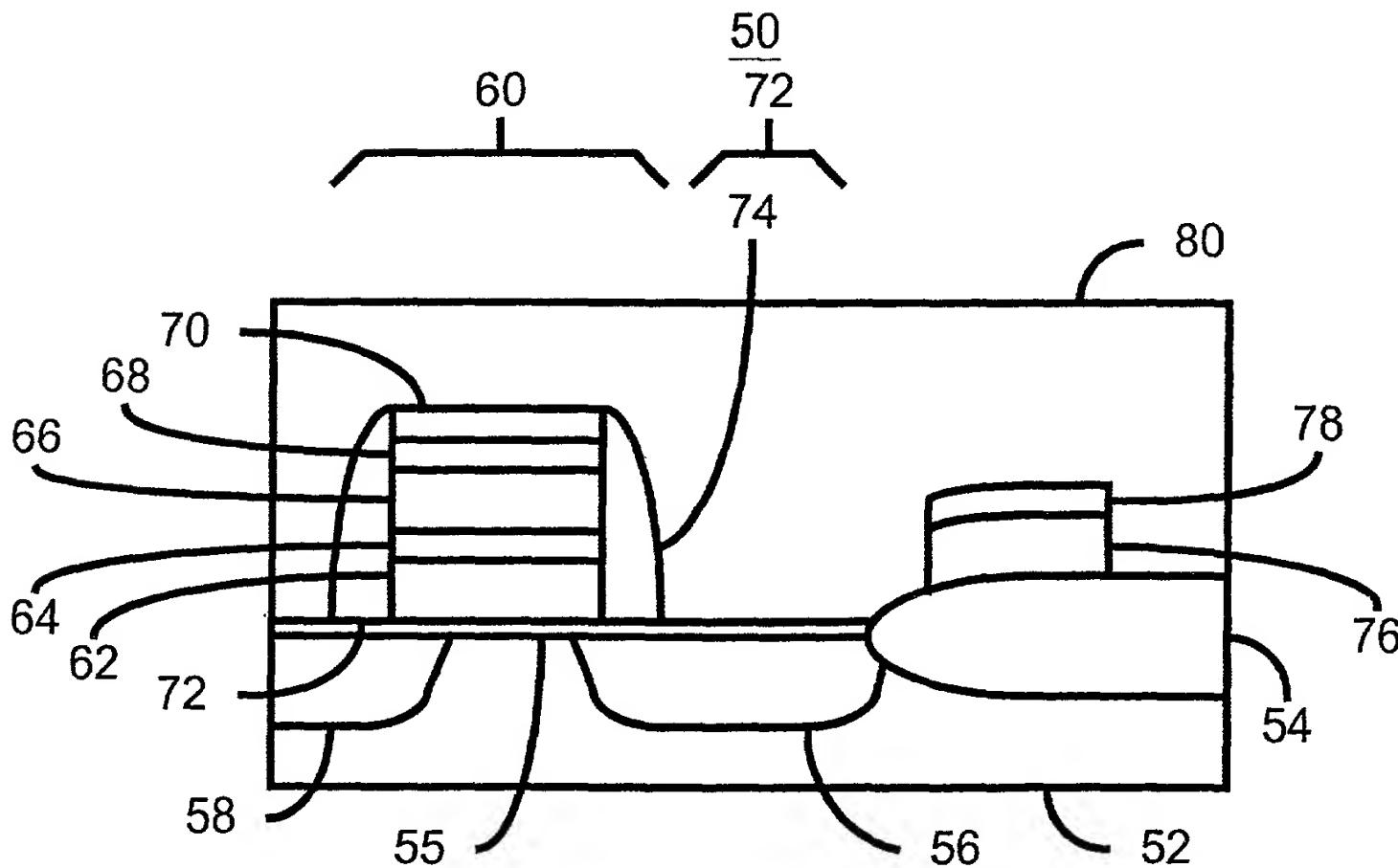
3 (a1) using a self-aligned silicide process to form the silicide on the top surface of
4 the polysilicon layer.

ABSTRACT

A method and system for providing at least one contact in a flash memory device is disclosed. The flash memory device includes a plurality of gate stacks and at least one component including a polysilicon layer as a top surface. The method and system further include forming a silicide on the top surface of the polysilicon layer and providing an insulating layer covering the plurality of gate stacks, the at least one component and the silicide. The method and system also include etching the insulating layer to provide at least one contact hole. The insulating layer etching step uses the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer. The method and system also include filling the at least one contact hole with a conductor.



Prior Art
Figure 1



Prior Art
Figure 2A

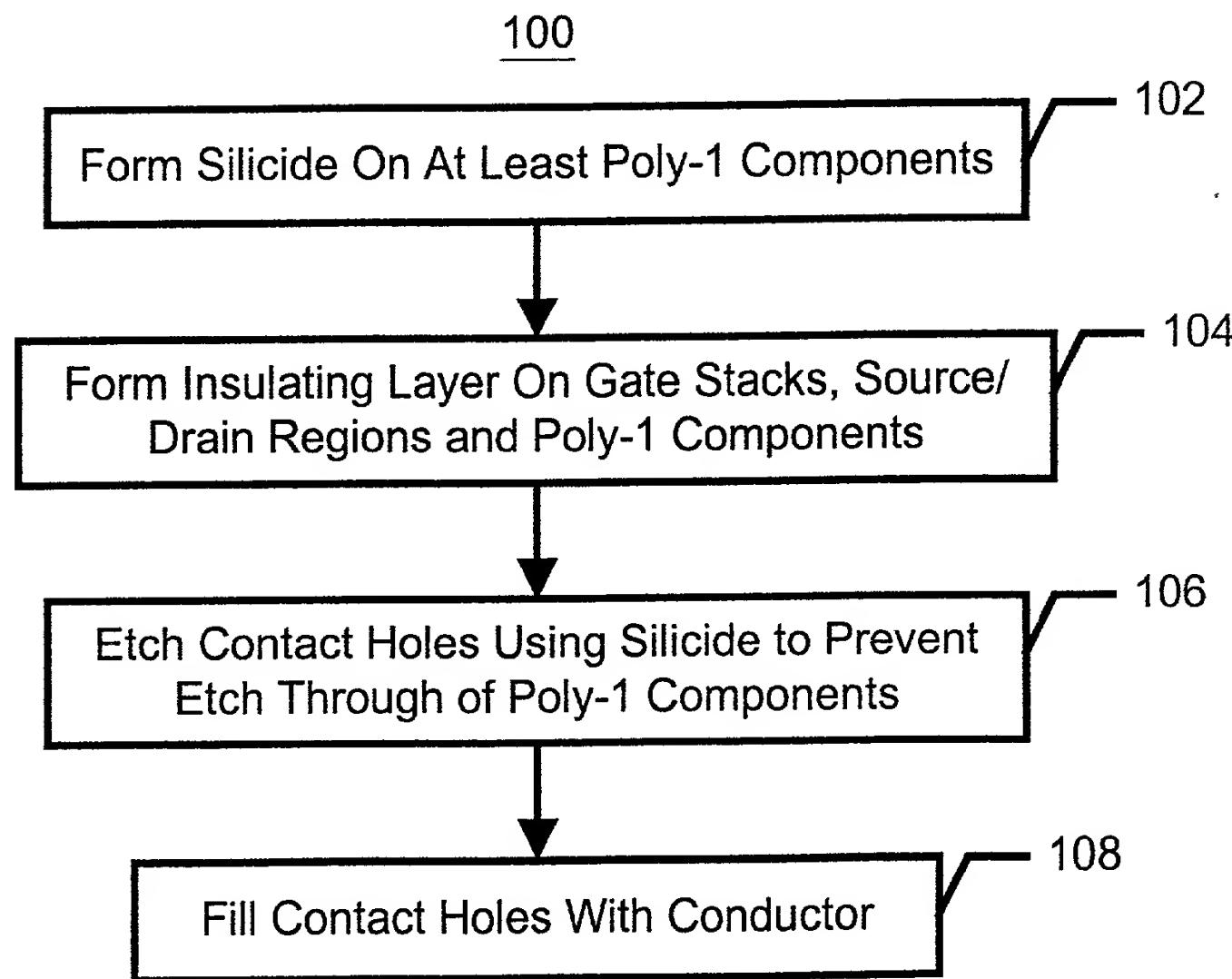
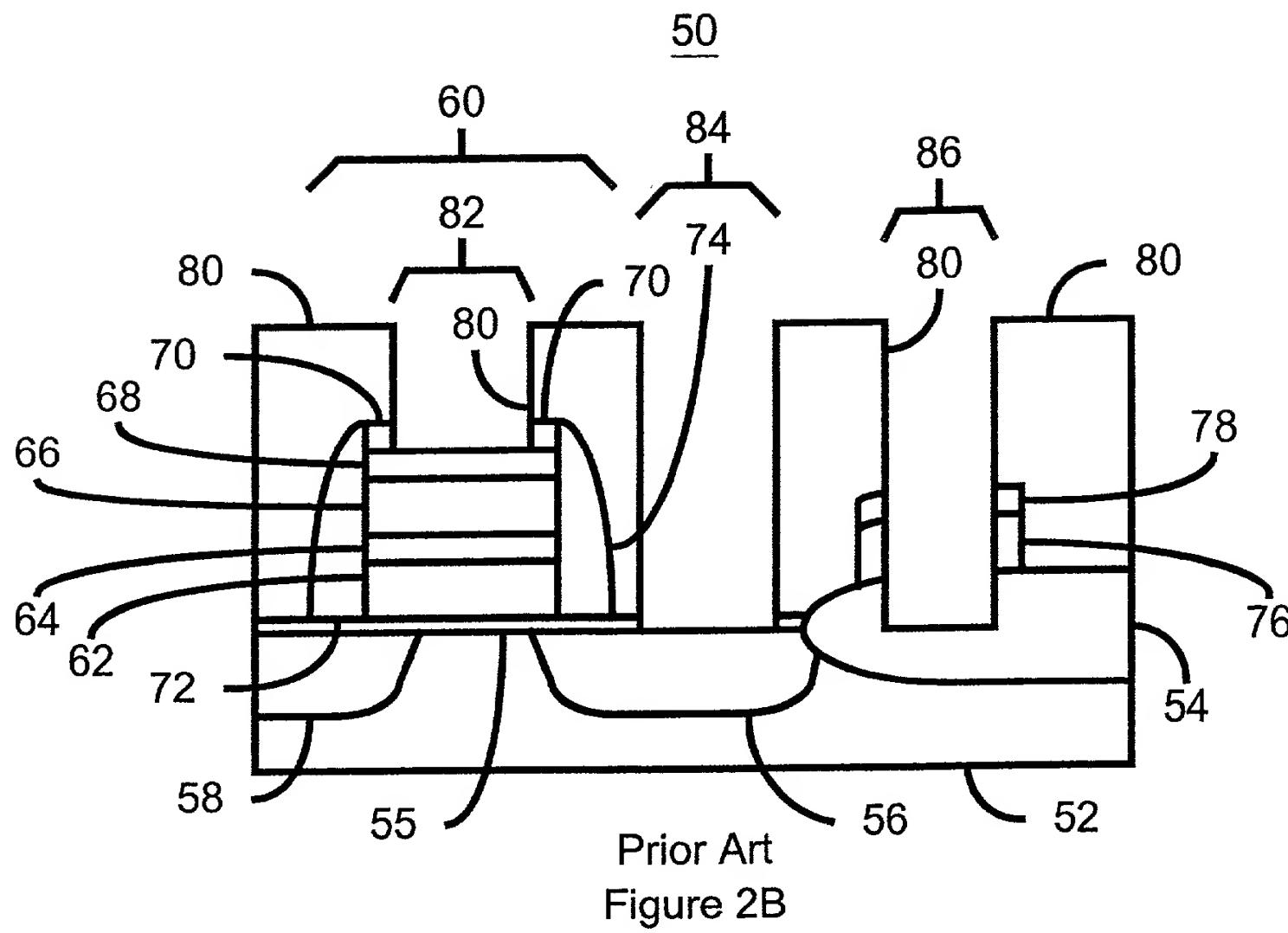


Figure 3A

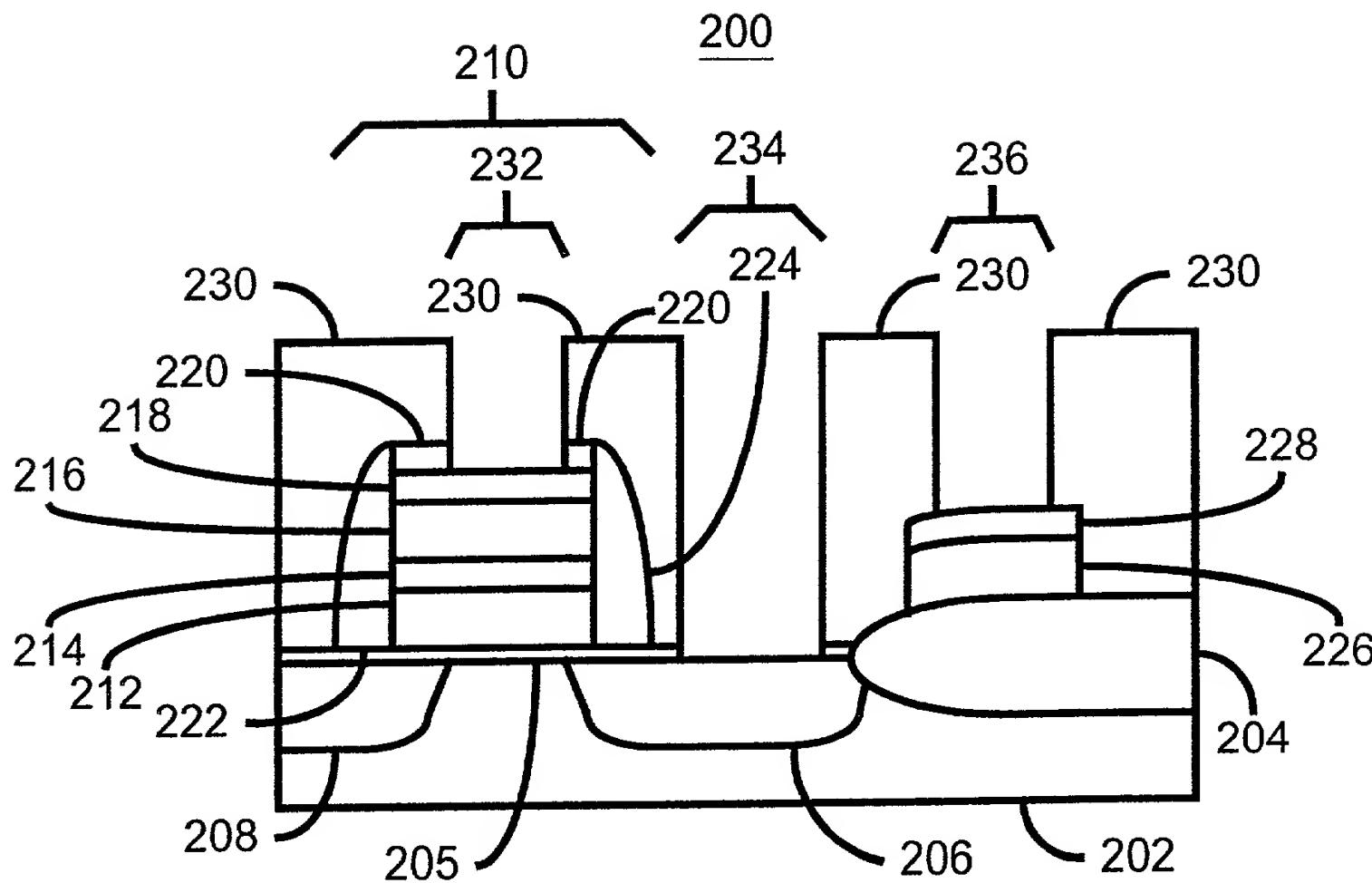


Figure 3B

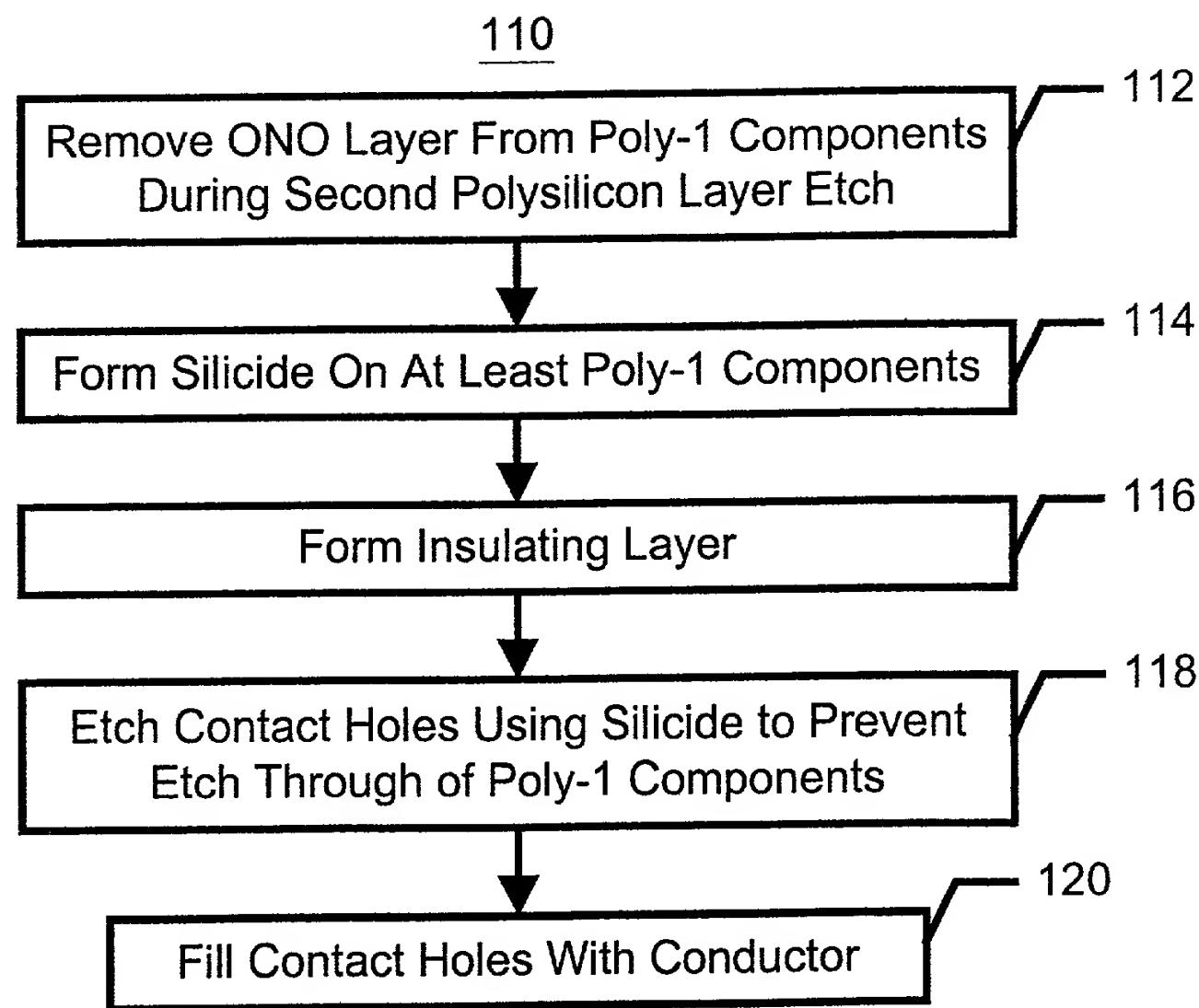


Figure 4

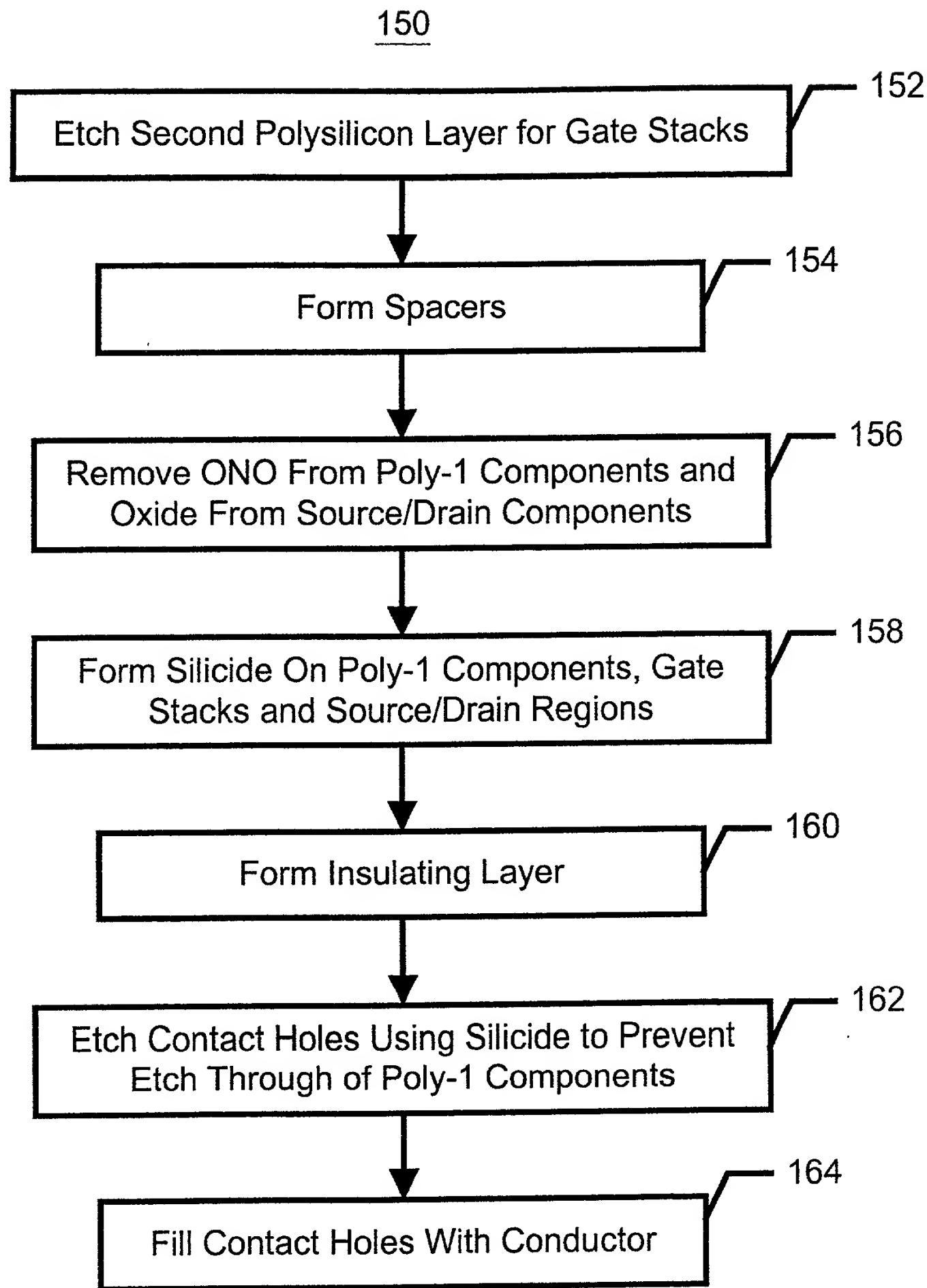


Figure 5A

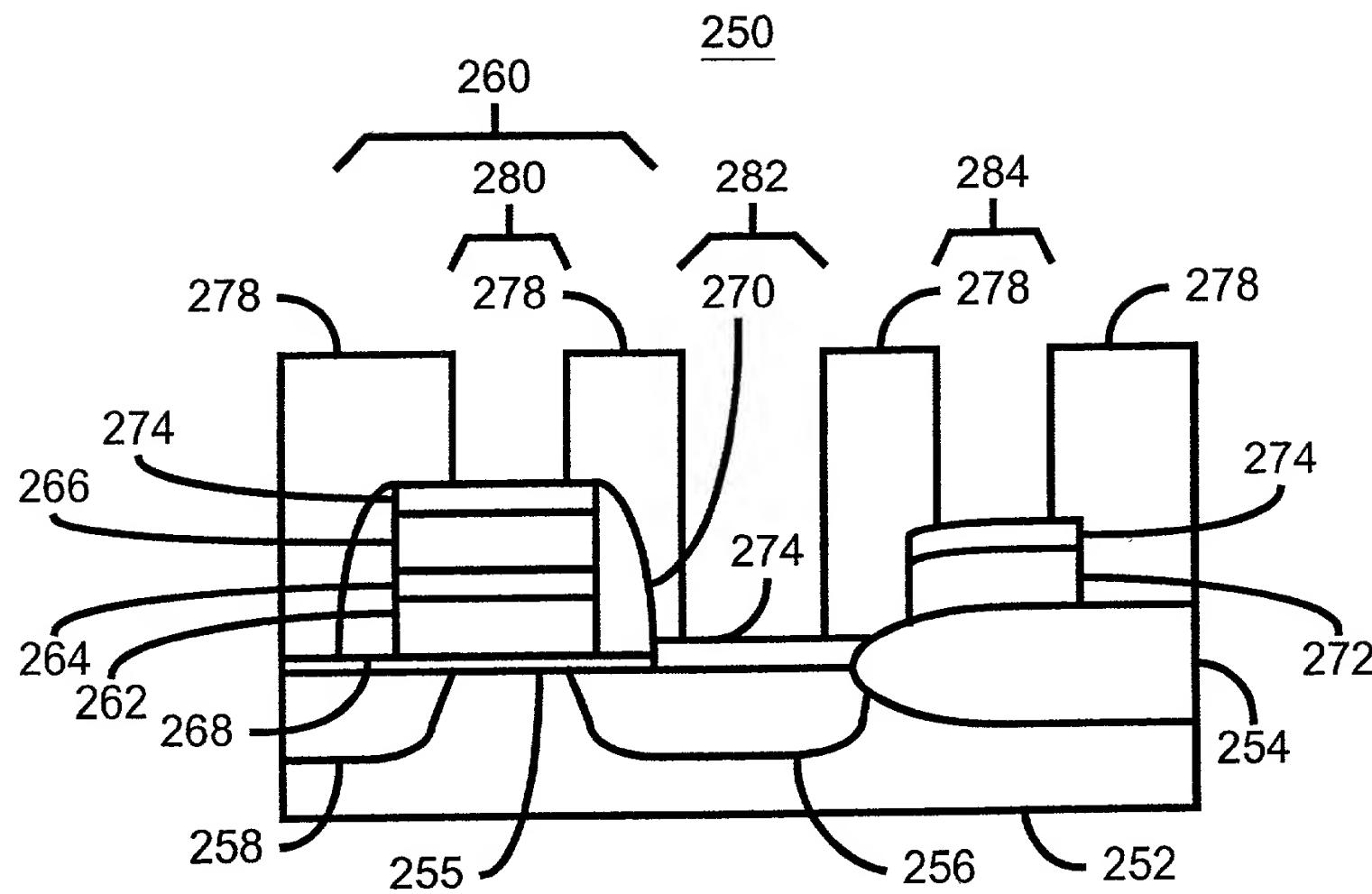


Figure 5B

DECLARATION

As the below named joint-inventors, we hereby declare that our residences, post office addresses and citizenships are as stated below next to our names; that we verily believe we are the first, original and joint-inventors of the invention entitled:

METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE

described and claimed in the specification which is attached hereto that we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; that we do not know and do not believe the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by us or our legal representatives or assigns more than twelve months prior to this application, that we acknowledge our duty to disclose information of which we are aware that is material to the examination of this application as defined by 37 C.F.R. 1.56, and that no application for patent or inventor's certificate on said invention has been filed in any country foreign to the United States of America by us or by our legal representatives or assigns.

Address all telephone calls to Mr. Sawyer at telephone number (650) 493-4540 and all correspondence to:

JOSEPH A. SAWYER JR.
SAWYER LAW GROUP LLP
P.O. Box 51418
Palo Alto, California 94303

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of first/joint Inventor: **Mark S. Chang**

Residence: **1881 Farndon Avenue**
Los Altos **Santa Clara** **California** **94024**
City **County** **State** **Zip**

Post Office Address: **Same as above**

Citizenship: **United States of America**

3/28/2000

Mark S. Chang
Signature of Inventor

DECLARATION (continued)

Name of second/joint Inventor: **Hao Fang**

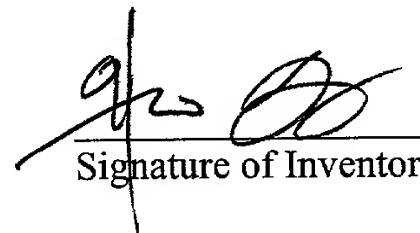
Residence: **7719 Carriage Circle**
Cupertino **Santa Clara** **California** **95014**
City **County** **State** **Zip**

Post Office Address: **Same as above**

Citizenship: **China, People's Republic of...**

2/23/2000

Date


Signature of Inventor

Name of third/joint Inventor: **King Wai Kelvin Ko**

Residence: **1717 Fumia Court**
San Jose **Santa Clara** **California** **95131**
City **County** **State** **Zip**

Post Office Address: **Same as above**

Citizenship: **Hong Kong**

3/17/00

Date


Signature of Inventor

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: **Mark S. Chang; Hao Fang; and King Wai Kelwin Ko**Title: **METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE****POWER OF ATTORNEY BY ASSIGNEE
AND EXCLUSION OF INVENTOR UNDER 37 C.F.R. SEC. 1.32**

Honorable Commissioner of Patents and Trademarks
 Box Patent Applications
 Washington, D.C. 20231

Sir:

ADVANCED MICRO DEVICES, Inc., a Delaware Corporation, having become the owner of all rights in and to the above-identified application by virtue of an Assignment executed by the inventor concurrently with the execution of the application, said Assignment being submitted herewith for recording, hereby appoints:

**Vincenzo D. Pitruzzella, Reg. No. 28,656
 Richard J. Roddy, Reg. No. 27,688
 William D. Zahrt, II, Reg. No. 26,070
 Paul S. Drake, Reg. No. 33,491
 Louis A. Riley, Reg. No. 39,817
 Elizabeth A. Apperley, Reg. No. 36,428**

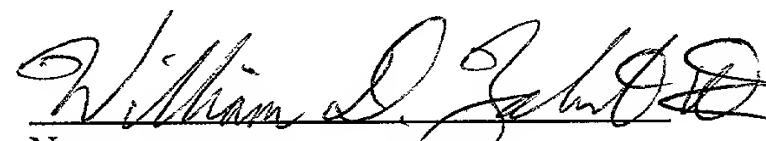
**Joseph A. Sawyer, Jr., Reg. No. 30,801
 Janyce R. Mitchell, Reg. No. 40,095
 Stephen G. Sullivan, Reg. No. 38,329
 Michele Liu, Reg. No. P44,875
 Wendell J. Jones, Reg. No. P45,961**

Please address all correspondence to:

**Joseph A. Sawyer, Jr.
 SAWYER LAW GROUP LLP
 P. O. Box 51418
 Palo Alto, CA 94303**

their attorneys, to prosecute said application and to transact in connection therewith all business in the Patent and Trademark Office and before competent International Authorities; said appointment to be to the exclusion of the inventor and his attorneys in accordance with the provisions of 37 C.F.R. 1.32.

Date: 29 March, 2000


 Name: WILLIAM D. ZAHRT II

Title: ASSISTANT GENERAL COUNSEL